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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/789,800	02/27/2004	Kevin Torek	303.871US1	5647

21186 7590 09/07/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 09/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/789,800	TOREK ET AL.	
	Examiner	Art Unit	
	Tu-Tu Ho	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *13 July 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-95* is/are pending in the application.

4a) Of the above claim(s) *46-95* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-45* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/09/2004 is acceptable.

Election/ Restriction

2. Applicant's election without traverse of Invention II, claims 1-45, in the reply filed on 07/13/2005 is acknowledged.

3. Claims 46-95 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 07/13/2005 as noted above.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. §103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. **Claims 1-37** are rejected under 35 U.S.C. §103(a) as being unpatentable over Shin et al. U.S. Patent 6,385,020 (the '020 reference) in view of Verhaverbeke et al. U.S. Patent 5,922,624.

Referring to **claims 1-16, 18-21, and 23-37**, the '020 reference discloses in Figs. 16A-16B and respective portions of the specification a memory device and an inherent method of

fabricating thereof comprising providing a semiconductor substrate (not shown, column 5, lines 60-65) that includes a memory container (generally defined by 120/130/140'/150) having a double-sided capacitor (generally defined by conductor/insulator/conductor 135/139/150 – Fig. 16A, that eventually becomes 137/142/151), which is functionally the same as the memory container having a double-sided capacitor of claim 1, functionally the same as the double-sided capacitor container of claims 7, 11, and 16, functionally the same as the memory container with a sidewall with an embedded capacitor of claim 21, functionally the same as the memory container whose side wall includes a double-sided capacitor of claim 26, and functionally the same as the double-sided container on a semiconductor substrate of claim 31; and etching a layer (130), that could be an oxide layer or a borophosphosilicate glass (BPSG) material (column 6, lines 15-30), the layer adjacent to the sidewall of the memory container, which is also the sidewall of the double-sided capacitor, or adjacent to the double-sided container.

However, the '020 reference fails to teach that the etching is a vapor phase etching as claimed. The reference thus further fails to teach that the vapor phase etching includes a vapor that includes hydrogen fluorine (HF), an alcohol, a methanol, and specially carboxylic that could functions as a surface tension lowing agent (claim 1) or as an etch initiator (claims 6, 11).

Verhaverbeke, in disclosing a method for semiconductor processing, teaches that a vapor phase etching including a vapor that includes hydrogen fluorine (HF), an alcohol, a methanol, and specially carboxylic - that could functions as a surface tension lowing agent or as an etch initiator as claimed, yields a much more uniform and reproducible product (columns 2-6, particularly column 2, lines 36-43, column 5, lines 16-18, and Tables 1-5, more particularly column 5, lines 16-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's semiconductor memory device using a vapor phase

etching as claimed. One would have been motivated to utilize such a vapor phase etching including a vapor that includes hydrogen fluorine (HF), an alcohol, a methanol, and specially carboxylic - that could functions as a surface tension lowing agent or as an etch initiator - in view of the teachings in Verhaverbeke that such a vapor phase etching yields a much more uniform and reproducible product.

Referring to **claims 17 and 22**, Verhaverbeke further teaches heating the etching material as claimed (column 5, last paragraph).

5. **Claims 38-45** are rejected under 35 U.S.C. §103(a) as being unpatentable over Shin et al. U.S. Patent 6,385,020 (the '020 reference) in view of Yang et al. U.S. Patent 6,727,155.

Referring to **claims 38 and 41-42**, the '020 reference discloses in Figs. 16A-16B and respective portions of the specification a memory device and an inherent method of fabricating thereof substantially as claimed and as detailed above for claims 1-37, including etching or removing the insulating layer (130, that could be BPSG or an oxide) but fails to disclose that the etching is a vapor wet etching operation.

Yang, in disclosing a method for forming a semiconductor device, teaches that a vapor wet etching is superior than a conventional etching in that the vapor wet etching prevents damages from occurring to the adjacent material layer, which is the source/drain regions in the Yang case (Yang, column 4, lines 23-26) and which would be the layer 135/120/100/semiconductor substrate in the '020 reference case (the '020 reference, Fig. 16A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '020 reference's semiconductor device using a vapor wet

etching. One would have been motivated to utilize such a vapor wet etching in view of the teachings in Yang that such a vapor wet etching prevents damages from occurring to an adjacent material layer.

Referring to claims 39-40 and 43-45, although both the '020 reference and Yang are quiet about the etching materials as claimed, the materials as claimed were known and available to one of ordinary skill in the art at the time the invention was made, for example, disclosed by Verhaverbeke as detailed above, therefore selection of such materials would have been obvious.

6. **Claims 1-37** are rejected under 35 U.S.C. §103(a) as being unpatentable over Thakur et al. U.S. Patent 6,251,720 (the '720 reference, and note the effective U.S. Publication date of the reference) in view of Verhaverbeke et al. U.S. Patent 5,922,624.

Referring to **claims 1-16, 18-21, and 23-37**, the '720 reference discloses in Fig. 1A and respective portions of the specification a memory device and an inherent method of fabricating thereof comprising providing a semiconductor substrate (101) that includes a memory container (generally indicated as 100, column 6, lines 47-50, for the label "container") having a double-sided capacitor (column 5, lines 55-60, generally defined by conductor//insulator//conductor 122/104//102//106, column 7, lines 12-18 and column 8, lines 58-60), which is functionally the same as the memory container having a double-sided capacitor of claim 1, functionally the same as the double-sided capacitor container of claims 7, 11, and 16, functionally the same as the memory container with a sidewall with an embedded capacitor of claim 21, functionally the same as the memory container whose side wall includes a double-sided capacitor of claim 26, and functionally the same as the double-sided container on a semiconductor substrate of claim 31; and (inherently) etching a layer (116), that could be an oxide layer or a borophosphosilicate glass (BPSG) material (column 7, lines 25-34), the layer adjacent to the

sidewall of the memory container, which is also the sidewall of the double-sided capacitor, or adjacent to the double-sided container (so as to form an opening to an area 108, for example).

However, the '720 reference fails to teach that the etching is a vapor phase etching as claimed. The reference thus further fails to teach that the vapor phase etching includes a vapor that includes hydrogen fluorine (HF), an alcohol, a methanol, and specially carboxylic that could functions as a surface tension lowing agent (claim 1) or as an etch initiator (claims 6, 11).

Verhaverbeke, in disclosing a method for semiconductor processing, teaches that a vapor phase etching including a vapor that includes hydrogen fluorine (HF), an alcohol, a methanol, and specially carboxylic - that could functions as a surface tension lowing agent or as an etch initiator as claimed, yields a much more uniform and reproducible product (columns 2-6, particularly column 2, lines 36-43, column 5, lines 16-18, and Tables 1-5, more particularly column 5, lines 16-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's semiconductor memory device using a vapor phase etching as claimed. One would have been motivated to utilize such a vapor phase etching including a vapor that includes hydrogen fluorine (HF), an alcohol, a methanol, and specially carboxylic - that could functions as a surface tension lowing agent or as an etch initiator - in view of the teachings in Verhaverbeke that such a vapor phase etching yields a much more uniform and reproducible product.

Referring to **claims 17 and 22**, Verhaverbeke further teaches heating the etching material as claimed (column 5, last paragraph).

7. **Claims 38-45** are rejected under 35 U.S.C. §103(a) as being unpatentable over Thakur et al. U.S. Patent 6,251,720 (the '720 reference, and note the effective U.S. Publication date of the reference) in view of Yang et al. U.S. Patent 6,727,155.

Referring to **claims 38 and 41-42**, the '720 reference discloses in Fig. 1A and respective portions of the specification a memory device and an inherent method of fabricating thereof substantially as claimed and as detailed above for claims 1-37, including inherently etching or removing the insulating layer (116, that could be BPSG or an oxide) but fails to disclose that the etching is a vapor wet etching operation.

Yang, in disclosing a method for forming a semiconductor device, teaches that a vapor wet etching is superior than a conventional etching in that the vapor wet etching prevents damages from occurring to the adjacent material layer, which is the source/drain regions in the Yang case (Yang, column 4, lines 23-26) and which would also be the source/drain regions 108 in the '720 reference case (Fig. 1A).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the '720 reference's semiconductor device using a vapor wet etching. One would have been motivated to utilize such a vapor wet etching in view of the teachings in Yang that such a vapor wet etching prevents damages from occurring to an adjacent material layer.

Referring to claims 39-40 and 43-45, although both the '720 reference and Yang are quiet about the etching materials as claimed, the materials as claimed were known and available to one of ordinary skill in the art at the time the invention was made, for example, disclosed by Verhaverbeke as detailed above, therefore selection of such materials would have been obvious.

Conclusion

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
September 03, 2005